

# High DR ADC for LHC

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# Status update: DRE+SAR+SEU

S.No.	Topic	Priority	Time required	To be tested by				Comments
				Jaro	Chen-Kai	Ray	Sarthak	
<b>System level testing</b>								
1a	Complete schematic at top level, create a testbench	1	By April 28th	x	x	x	x	
1b	Complete schematic DRC clear	1		95%	x	x	95%	Jaro: Check erc SK: Check density errors
1c	Complete schematic LVS clear			95%	x	x	x	Seal ring LVS remains
2	<b>Test clock timings</b>							
a	Clock to SAR, DRE, Scan Chain, Serializer in top level schematic, tt27.	1	0.5 days	90%	x	x	90%	Check driving capability and margins: Checked previously, need to recheck
b	Check DRE output (it should settle) and compare with the clock used for sampling by SAR block. Schematic level, tt 27	1	1 day	x	x	x	x	Check for timing margin
c	Check serializer clock in detail, synchronize with SAR outputs. Schematic, works on corner cases in schematic level	1	1 day	60%	x	x	20%	SK to make sure Decision bit stays valid at the end of load cycle.
			20					
3	Scan chain testing: Ability to drive bits. Check across corners, introducing intentional bit error and correction. Readout operation	1	1 day	x				
4	Driver and receiver: correct operation, with proper load? Across PVT?	1	0.5 days	10%				

# Status update: DRE+SAR+SEU

- Additional Simulations needed

S.No.	Topic	Priority	Time required	To be tested by				Comments
				Jaro	Chen-Kai	Ray	Sarthak	
4	Driver and receiver: correct operation, with proper load? Across PVT?	1	0.5 days	10%				
5	2 a, b, c testing in schematic, PVT	2	1 day	x	x	x	x	
6	2 a, b, c testing for tt 27, extracted view: different extraction corners	2	1 day	x	x	x	x	
7	Test shutting down DRE, outside input to SAR, test functionality. Schematic level, tt27	1	0.5 days	70%	x	x		Checked earlier. One scan chain problem is causing incorrect outputs currently. Working on it.
8	Test shutting down SAR, DRE to drive outside load, test functionality. Schematic level, tt27	1	0.5 days	70%			20%	Checked earlier. One scan chain problem is causing incorrect outputs currently. Working on it.
9	Turn off DRE, test SEU, Schematic level, tt 27	1	0.5 days			x		
10	Baseline shift test: See if able to get proper outputs Sch tt27	2					5%	SK: Awaiting basic correct sim from Jaro.

# Status update: DRE only top level

				To be tested by				
S.No.	Topic	Priority	Time required	Jaro	Chen-Kai	Ray	Sarthak	Comments
DRE testing on top schematics								
	COMPLETE TESTING			Jaro	Chen-Kai	Ray	Sarthak	
1	27 With all standard bits, test 1x, 4x, autoselect, test functionality outside chip. Schematic, tt	1	2 days				90%	Functionality means output should settle. SNDR > 65dB or so. Tested earlier, need retest
2	With all standard bits, test 1x, 4x, autoselect, test functionality using SAR. Schematic, tt 27	1	2 days	x			50%	Tested it once and it was working. Have to test it again since ChenKai did some modifications.
3	1, 2 testing across corners	3	2 days	x			50%	1 is tested individually with bond wires for all corners
4	1, 2 testing on extracted layouts	3	2 days	x			x	
5	Try running simulation with input of 20MSps. Outside the chip	3	2 days	50%			50%	Tested basic functionality, need to check for performance.
6	Same as 5, using SAR	3	2 days				20%	
7	Check 5 across corners	3					x	
8	Check 5 with extracted results	3					x	
9	Check 6 across corners	3					x	
10	Check 6 with extracted results	3					x	

# Status update: DRE only detailed

	VERSION 1 Testing: At DRE standalone level (with bondpads, bondwires etc.)			Jaro	Chen-Kai	Ray	Sarthak	
1	Schematic level testing at tt27 (trans SNDR)	1					x	
2	Schematic level testing at ff27, ss27, fs27, sf27 (trans SNDR)	1					x	Not meeting all requirements across corners, but simulations are done.
3	Schematic level testing at other corners (trans SNDR)	3					x	
4	Extraction level testing at tt27 (trans SNDR)	2					x	
5	Extraction level testing at ff27, ss27, fs27, sf27 (trans SNDR)	3					x	
6	Extraction level testing at other corners (trans SNDR)	4					x	
	VERSION 2			Jaro	Chen-Kai	Ray	Sarthak	
1	Schematics	1					x	
2	Layout	1					x	
	Phase 1: Testbench with real amplifier block, ideal clock gen							
1	AC dc simulations	1					x	
2	Trans Sinad simulations (tt, ss, ff, fs, sf) (-20, 80 degC)	1					x	Meets requirements at all corners, except ff80 (misses by 1dB)
	Phase 2: Testbench with real amplifier block, ideal clock gen							
1	AC dc simulations	1					20%	DC testbench not completely set (working on it).
2	Trans Sinad simulations (tt, ss, ff, fs, sf) (-20, 80 degC)	1					20%	Some of the simulations miss margins by 2dB. Esp ss80 and ff80
	Extractions on Phase 1 and Phase 2	2					x	5

# Conclusions from the updates

- DRE version 1:
  - Layout, DRC, LVS wise version 1 is 95% done
  - Testing wise: all priority 1 testing on version1 were complete. Currently facing a minor issue in scan chain. Should be resolved today.
  - Many level 2 priorities were addressed too.
- DRE version 2:
  - Schematics and basic testing done
  - Layout to be started.
  - Plan to complete by Monday latest.

# How difficult would be the transfer?

- DRE Version 1 -> DRE Version 2:
  - If done, only needs a redirect of library pointer
  - ~s.kalani/cadence6/01\_dreBlock/DRE\_SAR\_SEU\_sk -> ~/s.kalani/cadence6/04\_dreBlock\_stableAmp/DRE\_SAR\_SEU\_sk
  - (This is just an example, exact files to be shared later).

# Next steps

- Top level testing for v1: Complete
- Layout of DRE v2
- More testing on v2

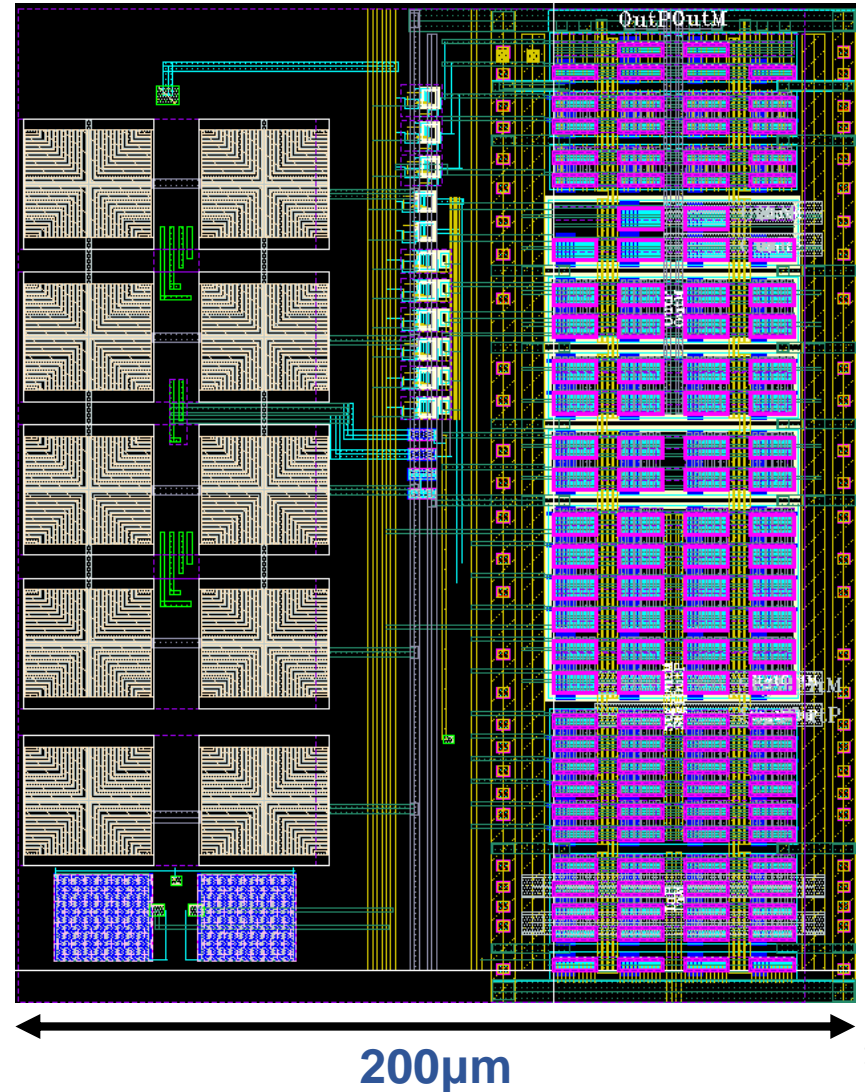
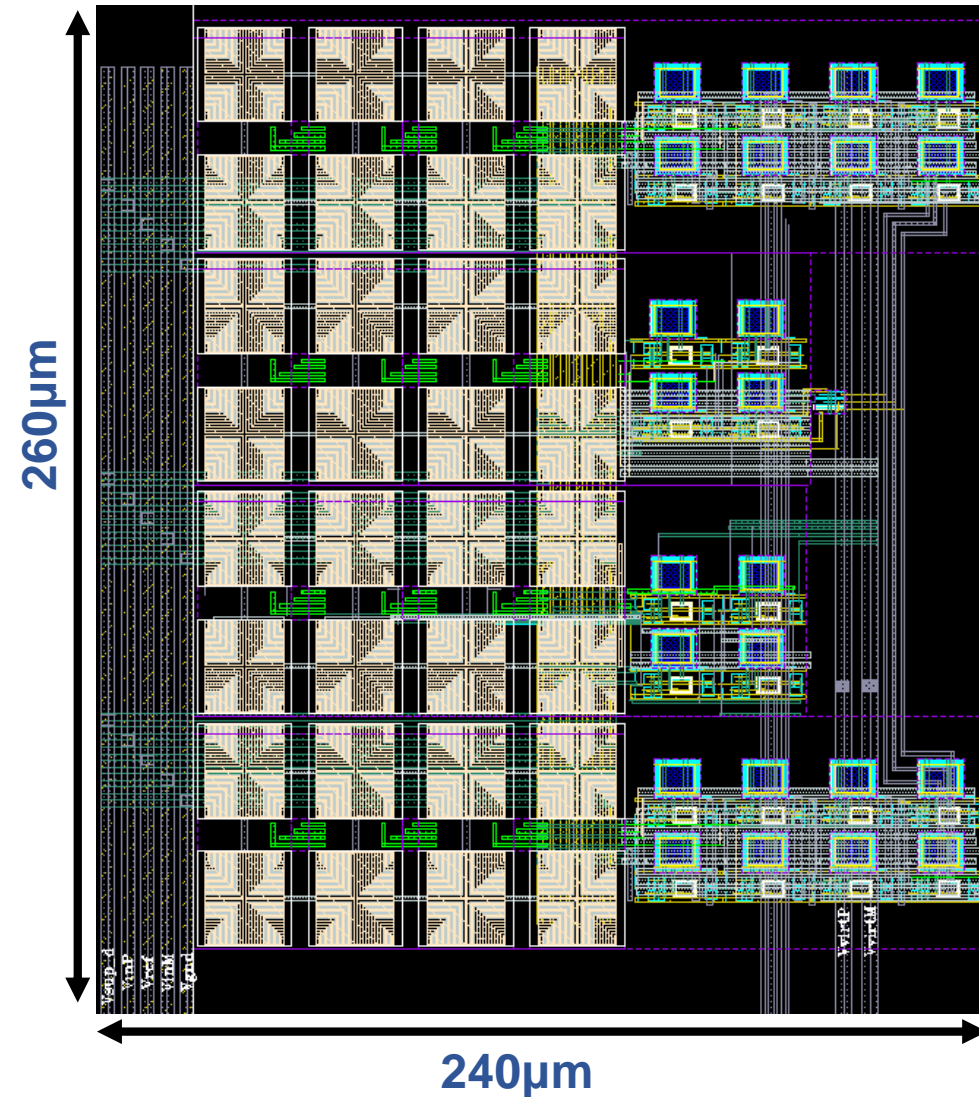
# Backup Slides

# Simulation Results

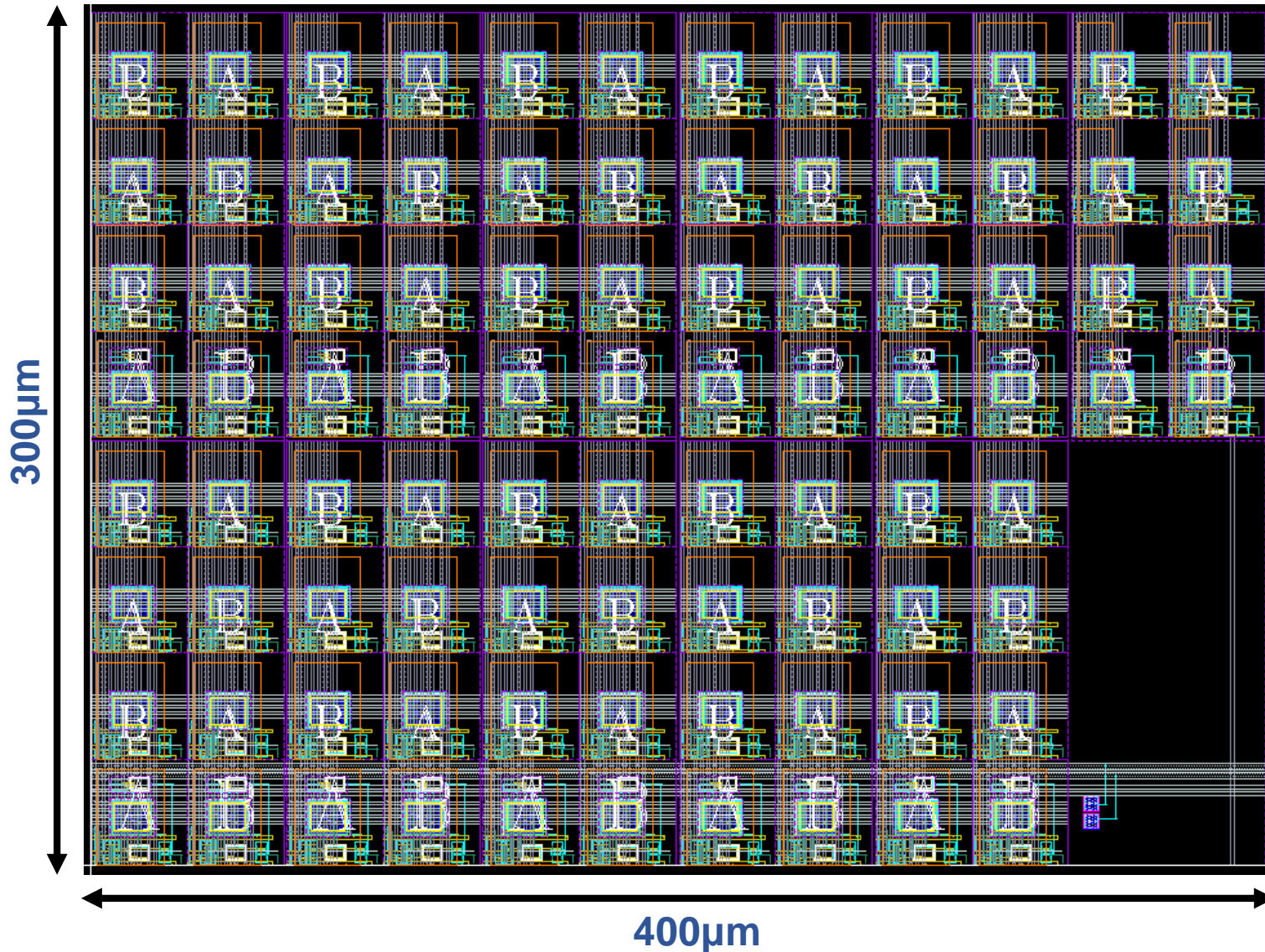
- Simulation done at DRE block schematic level, with bondwires (4nH), outputs taken externally, loading with 2pF (single ended).
- Autoselect used in all simulations. Vfs = 1.6Vpp assumed. I = 12mA to 21mA

Input Freq	Input Amp (diffpp)	Ideal SNDR (for current architecture)	CERN SNDR required (including 10dB margin)	tt27	ss27	ff27	fs27	sf27
4.844M	0.2V	67dB	>52dB	66.76	59.62	65.99	66.97	66.78
	0.4V	73dB	>54dB	66.51	62.41	64.2	62.25	68.65
	0.8V	73dB	>58dB	68.88	65.55	53.28	63.52	70.57
	1.6V	73dB	>60dB	73.85	69.8	60.04	70.55	74.22
19.84M	0.2V	67dB	>52dB	66.86	57.27	66.01	66.62	66.42
	0.4V	73dB	>54dB	70.32	59.7	66.65	69.11	68.65
	0.8V	73dB	>58dB	67.77	66	53.91	63.44	70.03
	1.6V	73dB	>60dB	66.44	60.04	63.15	66.96	70

# Sampling network and Differential Amplifier



# Miller Compensation Capacitor



# Clock Generator, Comparator & CLU

